MULTI-PURPOSE DIGITAL FREQUENCY SYNTHESIZER CIRCUIT FOR A PROGRAMMABLE LOGIC DEVICE

ABSTRACT

A digital frequency synthesizer (DFS) circuit adds little additional delay on the clock path. True and complement versions of an input clock signal are provided to a first and second passgates, respectively. Under the direction of a control circuit, the passgates pass selected rising edges of the true clock signal, and selected falling edges of the complement clock signal, to an output clock terminal of the DFS circuit. When neither the true nor the complement clock signal is passed, a keeper circuit retains the value already present at the output clock terminal. In some embodiments, both passgates can be disabled and a ground or power high signal can be applied to the output terminal. Other embodiments include PLDs in which the DFS circuits are employed to allow individual clock control for each programmable logic block.